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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/735,005	12/12/2000	Kazuyuki Ito	NEC 444	3384
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7590	06/16/2004
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EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/735,005

Applicant(s)

ITO, KAZUYUKI

Examiner

Samuel A Gebremariam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 08 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 37-40 and 42-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 37-40 and 42-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment filed 4/8/2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claim 42 recites the limitation "forming a grid-shaped trench" in line 4. However there is no support for grid-shaped trench in the specification as originally filed.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 42-44, 46 and 47 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 42 recites the limitation "forming a grid-shaped trench" in line 4. However there is no support for grid-shaped trench in the specification as originally filed. Therefore the claim is not described in the specification in such a way as to reasonably

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convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 46 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 46 recites the limitation "said dummy gates having a shape that is relative to a portion of said element isolation region" in lines 2 and 3. The scope of the claim is unclear as to what it means.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 37 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Gilbert US patent No. 5,885,856.

Regarding claim 37 admitted prior art teaches (figs. 3A-3C and 4) a method for manufacturing a semiconductor device comprising the steps of: forming a conductive layer (202) over the semiconductor substrate (201) forming a photoresist pattern layer on the conductive layer using a photomask having gate patterns (P1) and (P2) corresponding to the active areas and dummy gate patterns (DP) corresponding to the

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dummy areas and patterning the conductive layer by an etching process using the photoresist pattern.

Admitted prior art does not disclose forming a first photoresist pattern layer, a first photomask and forming a trench in the semiconductor substrate by an etching process using the first photoresist pattern layer.

It is conventional and well known to form isolation trench using photolithographic process. Gilbert also teaches (fig. 1, col. 2, lines 41-60) forming isolation trench (13) and burying insulating layer in the trenches and using masking layer (12) between active areas (14) and dummy regions (20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the first masking process for forming trench isolation trench structure taught by Gilbert in the process of admitted prior art in order to form isolation structures between the active region before forming the gate and dummy gate structures. Furthermore the combined process of admitted prior art and Gilbert results in a structure where each of the dummy gate patterns having a reduced area of the respective one of the dummy area patterns.

Regarding claims 39 and 40 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the dummy areas and or dummy gates are arranged in at least two rows and/ or two columns and the row is shifted from another and the row and/ or at least one column is shifted from another column.

It is conventional and also taught by Gilbert (fig. 6 and 7) arranging device structures in an array as claimed.

It would well within ordinary skill in the art to arrange the dummy gate and gate structures of admitted prior art device in the conventional manner in order to obtain high packing density.

7. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Gilbert and in further view of Shimomura et al. US patent No. 6,140,687.

Regarding claim 38 admitted prior art teaches substantially the entire claimed method of claim 37 above except explicitly stating that the shape of the dummy area and/ or dummy gate is a circle.

It is conventional and also taught by Shimomura forming circular shaped gates.

It would be well within ordinary skill in the art to select circular shape dummy/gate structures since circular structures allow for symmetrical arrangement of integrated circuit layout. Furthermore since it is known to form circular shaped gate electrodes it would have been obvious to form circular dummy gate electrode.

8. Claims 42-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert US patent No. 5,885,856 in view of admitted prior art.

Regarding claim 42, Gilbert teaches a method of manufacturing a semiconductor device, comprising: performing a selective etching on a semiconductor substrate (11) having first and second active areas (14) and an isolation area (13) intervening between the first and second active areas, thereby forming a grid-shaped trench (13) in the

isolation area of the semiconductor substrate to define a plurality of dummy regions (20) each surrounded by the grid-shaped trench; forming an insulating layer (15) in the grid-shaped trench.

Gilbert does not teach forming a conductive layer on the semiconductor substrate; and selectively removing the conductor layer to form a transistor gate over each of the first and second active areas and a dummy gate over each of the dummy regions, the dummy gate having a reduced shape area as compared to a shape area of a corresponding one of said dummy regions.

Admitted prior art teaches (fig. 3A-3C) forming a conductive layer (202) on the semiconductor substrate and selectively removing the conductor layer to form a transistor gate over a first and second active areas and a dummy gate (DP) over a dummy regions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the transistor and dummy gate structures taught by admitted prior art in the process of Gilbert in order to form an integrated structure with no dishing problem.

Furthermore the combined process of admitted prior art and Gilbert results in a structure where each of the dummy gate patterns having a reduced area of the respective one of the dummy area patterns.

Regarding claim 43, Gilbert teaches substantially the entire claimed process of claim 42 above including the insulating layer is formed by chemical mechanical polishing process (col. 2, lines 41-51).

Regarding claim 44, Gilbert teaches substantially the entire claimed process of claim 42 above including transistor gate and the dummy gate are formed by use of such a mask pattern that is derived by combining a transistor gate pattern and a dummy gate pattern which is obtained by reducing a mask pattern for forming the grid shaped trench.

Regarding claim 45, Gilbert teaches substantially the entire claimed process of claim 42 above including forming two or more dummy gates over the element isolation region between the first and the second gate electrodes (see figs. 3A-3C APA).

Regarding claim 46, Gilbert teaches substantially the entire claimed process of claim 42 above including the element isolation region includes a grid-shaped trench, and each of the dummy gates having a shape and the element isolation region surrounded by the grid-shaped trench.

Regarding claim 46, Gilbert teaches substantially the entire claimed process of claim 42 above including each of the dummy gates has a shape that is reduced as compared to the portion of the element isolation region.

Response to Arguments

9. Applicant's arguments filed 4/8/04 have been fully considered but they are not persuasive. Applicant argues that Gilbert does not teach using a first masking layer defining a trench which partitions pattern areas corresponding to active regions and dummy regions, using the masking layer in an etch step to form trenches in semiconductor substrate. As shown in figure 1 of Gilbert the masking layer (12) defining a trench (13) which partitions pattern areas corresponding to active regions and dummy regions, using the masking layer in an etch step to form trenches in semiconductor

substrate. Therefore the combined process of admitted prior art and Gilbert results in a two masking layers required to form the active and dummy regions.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4:30pm.

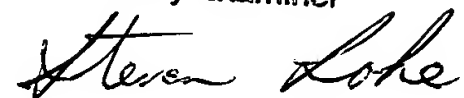
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
June 14, 2004

Steven Loke
Primary Examiner

A handwritten signature in black ink, appearing to read "Steven Loke", written in a cursive style.